WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

a plurality of field effect transistors formed in said semiconductor region;

power supply wirings for supplying the power supply voltages to a plurality of said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings,

wherein said switch elements are arranged discretely within said semiconductor region.

2. A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

a plurality of field effect transistors formed in said semiconductor region;

power supply wirings for supplying the power supply voltages to a plurality of said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings,

wherein said semiconductor region is provided with a semiconductor region of the conductivity type opposing to that of said semiconductor region and such semiconductor region and said power supply wirings are

electrically connected.

3. A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

a plurality of field effect transistors formed in said semiconductor region;

power supply wirings for supplying the power supply voltages to a plurality of said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings,

wherein at least one of a pair of semiconductor regions for source and drain of unused field effect transistors among a plurality of said field effect transistors and said power supply wirings are electrically connected.

4. A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

a plurality of field effect transistors formed in said semiconductor region;

power supply wirings for supplying the power supply voltages to a plurality of said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings,

wherein a plurality of switch elements are

discretely arranged within said semiconductor region, said semiconductor region is provided with a semiconductor region of the conductivity type opposed to that of said semiconductor region and said semiconductor region and power supply wirings are electrically connected.

5. A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

a plurality of field effect transistors formed in said semiconductor region;

power supply wirings for supplying the power supply voltages to a plurality of said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings,

wherein a plurality of said switch elements are discretely arranged in said semiconductor region and at least one of a pair of semiconductor regions for source and drain of unused field effect transistors among a plurality of said field effect transistors and said power supply wirings are electrically connected.

6. A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

a plurality of field effect transistors formed in said semiconductor region;

power supply wirings for supplying the power supply voltages to a plurality of said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings,

wherein said switch elements are discretely arranged within said semiconductor region, a semiconductor region of the conductivity type opposes to that of said semiconductor region is provided between the switch elements discretely arranged in said semiconductor region and such semiconductor region and said power supply wirings are electrically connected.

7. A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

a plurality of basic cells regularly arranged on said semiconductor substrate;

a plurality of field effect transistors arranged in each of a plurality of said basic cells and formed in said semiconductor region;

power supply wirings for supplying the power supply voltages to a plurality of said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings;

wherein said switch elements are formed of the field effect transistors in said basic cells and are

discretely arranged in said semiconductor region.

Sub C33

8. A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

a plurality of basic cells regularly arranged in said semiconductor substrate;

a plurality of field effect transistors arranged in each of a plurality of said basic cells and formed in said semiconductor region;

power supply wirings for supplying the power supply voltages to said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings,

wherein said switch elements are formed of field effect transistors of said basic cells and a semiconductor region, which is formed within said semiconductor region in a plurality of said basic cells, of the conductivity type opposed to that of said semiconductor region and said power supply wirings are electrically connected.

9. A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

a plurality of basic cells regularly arranged on said semiconductor substrate;

a plurality of field effect transistors arranged in each of a plurality of basic cells and are formed

in said semiconductor region;

power supply wirings for supplying the power supply voltages to said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings,

wherein said switch elements are formed of the field effect transistors of said basic cells and at least one of a pair of semiconductor regions for source and drain of unused field effect transistors of said field effect transistors and said power supply wirings are electrically connected.

10. A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

a plurality of basic cells regularly arranged in said semiconductor substrate;

a plurality of field effect transistors arranged in each of a plurality of said basic cells and formed in said semiconductor region;

power supply wirings for supplying the power supply voltages to said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings,

wherein said switch elements are formed of said field effect transistors of basic cells and are discretely arranged within said semiconductor region, and

wherein a semiconductor region, formed in said semiconductor region of a plurality of said basic cells, of the conductivity type opposed to that of said semiconductor region and said power supply wirings are electrically connected.

11. A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

a plurality of basic cells regularly arranged in said semiconductor substrate;

a plurality of field effect transistors arranged in each of a plurality of said basic cells and are formed in said semiconductor region;

power supply wirings for supplying the power supply voltages to said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings,

wherein said switch elements are formed of said field effect transistors of basic cells and are discretely arranged within said semiconductor region, and

wherein at least one of a pair of semiconductor regions for source and drain of unused field effect transistors of said field effect transistors and said power supply wirings are electrically connected.

12. A semiconductor device, comprising:

a semiconductor region formed in a semiconductor

substrate;

a plurality of basic cells regularly arranged in said semiconductor substrate;

a plurality of field effect transistors arranged in each of a plurality of said basic cells and formed in said semiconductor region;

power supply wirings for supplying the power supply voltages to said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings,

wherein said switch elements are formed of said field effect transistors of basic cells and are discretely arranged in said semiconductor region, and

wherein at least one of a pair of semiconductor regions for source and drain of unused field effect transistors arranged between the switch elements discretely arranged in said semiconductor region among said field effect transistors and said power supply wirings are electrically connected.

13. A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

a plurality of basic cells regularly arranged in said semiconductor substrate;

a plurality of field effect transistors arranged in each of a plurality of said basic cells and formed in said semiconductor region;

circuits formed of a plurality of said basic cells;

power supply wirings for supplying the power supply voltages to said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings,

wherein said switch elements are built in the predetermined circuit among said circuits.

14. A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

a plurality of basic cells regularly arranged in said semiconductor substrate;

a plurality of field effect transistors arranged in each of a plurality of said basic cells and formed in said semiconductor region;

circuits formed of a plurality of said basic cells;

power supply wirings for supplying the power supply voltages to said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings,

wherein said circuits include the circuit to which said switch elements are built in and the circuit to which said switch elements are not built in.

15. A semiconductor device as claimed in claim 13 or 14, wherein a semiconductor region, of the conductivity type opposed to that of said semiconductor region, formed in said semiconductor region of a plurality of

said basic cells and said power supply wirings are electrically connected.

16. A semiconductor device as claimed in claim 13 or 14, wherein at least one of a pair of semiconductor regions for source and drain of unused field effect transistors among said field effect transistors and said power supply wirings are electrically connected.

17. A semiconductor device as claimed in any one of claims 13 to 16, wherein said circuits are logic circuits and said switch elements are discretely arranged in said semiconductor substrate.

18. A semiconductor device as claimed in claim 16, wherein said unused field effect transistors are field effect transistors of basic cells not forming logic circuits and said unused basic cells are formed among said switch elements.

19. A semiconductor device as claimed in any one of claims 13 to 18, wherein said circuit comprising the switch elements is a clock circuit or a flip-flop circuit.

20. A semiconductor device as claimed in any one of claims 13 to 19, wherein said switch elements are formed of field effect transistors in said basic cells.

21. A semiconductor device as claimed in any one of claims 7 to 20, wherein said basic cells include the p-channel type field effect transistors and n-channel type field effect transistors.

22. A semiconductor device as claimed in any one of claims 7 to 12 or 20, wherein a wiring electrically connected to the gate electrode of said switch element is formed of the wiring of the third wiring layer and this wiring is arranged in parallel to said power supply wirings.

23. A semiconductor device as claimed in any one of claims 7 to 22, wherein a semiconductor region for power feeding to supply the predetermined voltage to the semiconductor region formed in said semiconductor substrate is formed in the region between the internal circuit region where a plurality of said basic cells are arranged and the peripheral circuit region at the external side of said internal circuit region.

24. A semiconductor device as claimed in claim 23, wherein a wiring for supplying the predetermined voltage to said semiconductor region for power feeding is arranged to surround said internal circuit region.

25. A semiconductor device as claimed in claim 24, wherein the wiring for supplying the predetermined voltage to said semiconductor region for power feeding is electrically connected to the terminal for testing via the external terminal of the semiconductor device.

26. A semiconductor device as claimed in claim 24, wherein the wiring for supplying the predetermined voltage to said semiconductor region for power feeding is electrically connected to the wiring for power

feeding arranged like a lattice within said internal circuit region.

27. A semiconductor device as claimed in any one of claims 1 to 26, wherein said switch elements are turned ON in the normal operation period of semiconductor device and the power supply voltage is applied from said power supply wirings to the semiconductor region formed in said semiconductor substrate and said switch elements are turned OFF in the testing or waiting period of semiconductor device and the voltage different from said power supply voltage is applied to said semiconductor region.

28. A semiconductor device, comprising:

a first semiconductor region formed in a semiconductor substrate;

a plurality of basic cells regularly arranged in said semiconductor substrate;

a first field effect transistor formed in said first semiconductor region as the field effect transistor of said basic cells;

a second field effect transistor formed in said second semiconductor region as the field effect transistor of said basic cells to have the conductivity type opposed to that of said first field effect transistor;

a first power supply wiring connected to said first field effect transistor;

a second power supply wiring connected to said second field effect transistor to supply a potential which is relatively lower than the potential of said first power supply wiring;

first switch elements provided between said first semiconductor region and said first power supply wiring; and

second switch elements provided between said second semiconductor region and said second power supply wiring,

wherein said first switch elements are formed of the first field effect transistors in said basic cells and discretely arranged within said first semiconductor region, and

wherein said second switch elements are formed of the second field effect transistors in said basic cells and discretely arranged within said second semiconductor region.

29. A semiconductor device, comprising:

a first semiconductor region formed in a semiconductor substrate;

a second semiconductor region formed in said semiconductor substrate to have conductivity type opposed to that of said first semiconductor region;

a plurality of basic cells regularly arranged in said semiconductor substrate;

a first field effect transistor formed in said

first semiconductor region as the field effect transistor in said basic cells;

Sub C33

a second field effect transistor, as the field effect transistor in said basic cells, formed in said second semiconductor region to have the conductivity type opposed to that of said first field effect transistor;

a first power supply wiring connected to said first field effect transistor;

a second power supply wiring connected to said second field effect transistor to supply the potential which is relatively lower than that of said first power supply wiring;

a first switch element provided between said first semiconductor region and said first power supply wiring; and

a second switch element provided between said second semiconductor region and said second power supply wiring,

wherein said first switch element is formed of the first field effect transistor in the predetermined basic cells among a plurality of said basic cells,

wherein said second switch element is formed of the second field effect transistor in the predetermined basic cells among a plurality of said basic cells,

wherein the region formed in said first semiconductor region in a plurality of basic cells

electrically connects the semiconductor region of the conductivity type opposed to that of said first semiconductor region and said first power supply wiring, and

wherein the region formed in said second semiconductor region in a plurality of basic cells electrically connects the semiconductor region of the conductivity type opposed to that of said second semiconductor region and said second power supply wiring.

30. A semiconductor device, comprising:

a first semiconductor region formed in a semiconductor substrate;

a second semiconductor region formed in said semiconductor substrate to have conductivity type opposed to that of said first semiconductor region;

a plurality of basic cells regularly arranged in said semiconductor substrate;

a first field effect transistor formed in said first semiconductor region as the field effect transistor of said basic cells;

a second field effect transistor, as the field effect transistor of said basic cells, formed in said second semiconductor region to have the conductivity type opposed to that of said first field effect transistor;

a first power supply wiring connected to said first

effect transistor;

a second power supply wiring connected to said second field effect transistor to supply the potential relatively lower than that of said first power supply wiring;

a first switch element provided between said first semiconductor region and said first power supply wiring; and

a second switch element provided between said second semiconductor region and said second power supply wiring,

wherein said first switch element is formed of the first field effect transistor in the predetermined basic cells among a plurality of said basic cells,

wherein said second switch element is formed of the second field effect transistor in the predetermined basic cells among a plurality of said basic cells,

wherein at least one of a pair of semiconductor regions for source and drain of unused first field effect transistors among said first field effect transistors is electrically connected to said first power supply wiring, and

wherein at least one of a pair of semiconductor regions for source and drain of unused second field effect transistors among a plurality of said field effect transistors is electrically connected said second power supply wiring.

Sub C33

31. A semiconductor device, comprising:

a first semiconductor region formed in a semiconductor substrate;

a second semiconductor region formed in said semiconductor substrate to have the conductivity type opposed to that of said first semiconductor region;

a plurality of basic cells regularly arranged in said semiconductor substrate;

a first field effect transistor formed in said first semiconductor region as the field effect transistor of said basic cell;

a second field effect transistor formed, as the field effect transistor of said basic cell, in said second semiconductor region to have the conductivity type opposed to that of said first field effect transistor;

a first power supply wiring connected to said first field effect transistor;

a second power supply wiring connected to said second field effect transistor to supply the potential relatively lower than that of said first power supply wiring;

a first switch element provided between said first semiconductor region and said first power supply wiring; and

a second switch element provided between said second semiconductor region and said second power

supply wiring,

wherein said first switch elements are formed of the first field effect transistors in the predetermined basic cells among a plurality of said basic cells and are discretely arranged in said first semiconductor region,

wherein said second switch elements are formed of the second field effect transistors in the predetermined basic cells among a plurality of said basic cells and are discretely arranged in said first semiconductor region,

wherein the region formed in said first semiconductor region in a plurality of said basic cells electrically connects the semiconductor region of the conductivity type opposed to that of said first semiconductor region and said first power supply wiring, and

wherein the region formed in said second semiconductor region in a plurality of said basic cells electrically connects the semiconductor region of the conductivity type opposed to that of said second semiconductor region and said second power supply wiring.

32. A semiconductor device, comprising:

a first semiconductor region formed in a semiconductor substrate;

a second semiconductor region formed in said

semiconductor substrate to have the conductivity type opposed to that of said first semiconductor region;

a plurality of basic cells regularly arranged in said semiconductor substrate;

a first field effect transistor formed in said first semiconductor region as the field effect transistor of said basic cells;

a second field effect transistor formed, as the field effect transistor of said basic cells, in said second semiconductor region to have the channel of the conductivity type opposed to that of said first field effect transistor;

a first power supply wiring connected to said first field effect transistor;

a second power supply wiring connected to said second field effect transistor to supply the potential relatively lower than that of said first power supply wiring;

a first switch element provided between said first semiconductor region and said first power supply wiring; and

a second switch element provided between said second semiconductor region and said second power supply wiring,

wherein said first switch elements are formed of the first field effect transistors in the predetermined basic cells among a plurality of basic cells and are

discretely arranged in said first semiconductor region,

wherein said second switch elements are formed of the second field effect transistors in the predetermined basic cells among a plurality of basic cells and are discretely arranged in said first semiconductor region,

wherein at least one of a pair of semiconductor regions for source and drain of unused first field effect transistors among a plurality of first field effect transistors is electrically connected to said first power supply wiring, and

wherein at least one of a pair of semiconductor regions for source and drain of unused second field effect transistors among a plurality of said field effect transistors is electrically connected to said second power supply wiring.

33. A semiconductor device, comprising:

first and second semiconductor regions formed in the peripheral circuit region of a semiconductor substrate;

a plurality of cells for input/output circuits regularly arranged in the peripheral circuit region of said semiconductor substrate;

a plurality of field effect transistors for input/output circuits arranged in each of a plurality of cells for input/output circuits and formed in said first and second semiconductor regions;

power supply wiring for supplying the power supply voltage to a plurality of said field effect transistors for input/output circuits; and

switch element provided between the second semiconductor region in said peripheral circuit region and said power supply wiring,

wherein an output circuit electrically connected to the external terminal is formed of the field effect transistors for input/output circuits in said first semiconductor region and an input circuit electrically connected to the external terminal is formed of the field effect transistors for input/output circuits in said second semiconductor region, and

wherein said switch elements are formed of the field effect transistors not used for the input circuit among the field effect transistors for input/output circuits in said second semiconductor region.

34. A semiconductor device, comprising:

a semiconductor region formed in the peripheral circuit region of a semiconductor substrate;

a plurality of cells for input/output circuits regularly arranged in the peripheral circuit region of said semiconductor substrate;

a plurality of field effect transistors for input/output circuits arranged in each of a plurality of cells for input/output circuits and formed in said semiconductor region;

power supply wiring for supplying the power supply voltage to a plurality of said field effect transistors for input/output circuits; and

switch element provided between the semiconductor region in said peripheral circuit region and said power supply wiring,

wherein said peripheral circuit region includes an external region to arrange said field effect transistors for input/output circuits of relatively higher threshold voltage and an internal region to arrange said field effect transistors for input/output circuits of relatively lower threshold voltage, and

wherein said switch element is formed of the field effect transistor not used for input circuit among the field effect transistors for input/output circuits in said internal region.

35. A semiconductor device as claimed in claim 34, wherein an output circuit is formed of the field effect transistor for input/output circuits in said external region and an input circuit is formed of the field effect transistor for input/output circuits in said internal region.

36. A semiconductor device as claimed in claim 33, 34 or 35, wherein the gate insulation film of the field effect transistor forming said output circuit is thicker than the gate insulation film of the field effect transistor forming said input circuit.

37. A semiconductor device as claimed in claim 33, 34, 35 or 36, wherein the wiring connected to the gate electrode of the field effect transistor forming said switch element is arranged to surround the internal circuit region of a semiconductor device.

38. A semiconductor device as claimed in any one of claims 33 to 37, wherein at least one of a pair of semiconductor regions for source and drain of the field effect transistors unused for said input/output circuits is electrically connected to said power supply wiring to form a capacitance element.

39. A method of manufacturing a semiconductor device, comprising the processes of:

(a) regularly allocating a plurality of basic cells on a semiconductor substrate;

(b) forming a switch element for electrically connecting or disconnecting the semiconductor region formed on said semiconductor substrate and the power supply wiring of the semiconductor device; and

(c) forming a plurality of circuits with the predetermined basic cells among a plurality of said basic cells.

40. A method of manufacturing a semiconductor device, comprising the processes of:

(a) regularly allocating a plurality of basic cells on a semiconductor substrate;

(b) forming a switch element for electrically

connecting and disconnecting the semiconductor region formed on said semiconductor substrate and the power supply wiring of semiconductor device with the field effect transistor of the predetermine basic cells among a plurality of said basic cells;

(c) forming a plurality of circuits with the predetermined basic cells among a plurality of said basic cells; and

(d) allocating a contact hole for electrically connecting at least one of a pair of semiconductor regions for source and drain of unused field effect transistors among a plurality of said basic cells and said power supply wiring.

41. A method of manufacturing a semiconductor device comprising the processes of:

(a) regularly allocating a plurality basic cells on a semiconductor substrate;

(b) forming a switch element for electrically connecting and disconnecting the semiconductor region formed on said semiconductor substrate and the power supply wiring of semiconductor device with the field effect transistor of the predetermined basic cells among a plurality of said basic cells; and

(c) forming a plurality of circuits with the predetermined basic cells among a plurality of basic cells,

wherein said switch element is built in the

predetermined circuit among a plurality of said circuits in said process (c).

42. A method of manufacturing a semiconductor device, comprising the processes of:

(a) regularly allocating a plurality of basic cells on a semiconductor substrate; and

(b) forming a plurality of circuits with the predetermined basic cells among a plurality of said basic cells,

wherein said switch element is built in the predetermined circuit among a plurality of said circuits.

43. A semiconductor device as claimed in claim 2, 4, 6 or 8, wherein a capacitance element is formed of said semiconductor region and a semiconductor region of the conductivity type opposed to that of said semiconductor region.

44. A semiconductor device as claimed in claim 3, 5, 9, 11 or 12, wherein a capacitance element is formed of said semiconductor region and at least one of a pair of semiconductor regions for source and drain of said unused field effect transistors.

45. A semiconductor device as claimed in any one of claims 7 to 12, 43 and 44, wherein a logic circuit is formed using said basic cells and said logic circuit is formed among the basic cells forming said switch element.

46. A semiconductor device claimed in claim 9, 11, 12, 44 or 45; wherein a logic circuit is formed using said basic cells, said unused field effect transistor is the field effect transistor of basic cell not forming a logic circuit and said logic circuit and unused basic cells are formed among the basic cells forming said switch element.